ASAP 2012 Program

Monday

Time	Duration	Section	Room	Title	Authors
8:00	1:00	**Registration**	Hallway		
9:00	0:05	**Opening**	Auditorium	**Welcome and Opening**	
9:05	0:45	**Keynote 1**	Auditorium	**Embedded Multicore Design Technologies: The Next Generation**	Rainer Leupers
9:50	0:50	**Coffee break**	Business Lounge	**Break + Poster Session I**	
10:40	1:15	**Reconfigurable Logic and Graphics Engines**			
10:40	0:00		Auditorium	**Real-Time Iris Segmentation on FPGA**	Hau Ngo, Jennifer Shafer, Robert Ives, Ryan Rakvic and Randy Broussard
10:40	0:25		Auditorium	**A Reconfigurable Computing Approach for Efficient and Scalable Parallel Graph Exploration**	Brahim Betkaoui, Yu Wang, David Thomas and Wayne Luk
11:05	0:25		Auditorium	**High Performance Parallel JPEG2000 Streaming Decoder Using GPGPU-CPU Heterogeneous System**	Roto Le, Joseph Mundy and Iris Bahar
11:30	0:25		Auditorium	**A Performance Model for Memory Bandwidth Constrained Applications on Graphics Engines**	Lin Ma and Roger Chamberlain
11:55	1:05	**Lunch**	Business Lounge		
13:00	5:00	**Special Session on Ongoing EU Projects**			Koen Bertels
13:00	1:45		Auditorium	**Cluster 1 Session: Presentations (Smecy, iFEST, 2Parma, ALMA, Faster, Reflect, Madness)**	
			Business Lounge	**Cluster 2 Session: Presentations (ERA, DeSyRe, EPICS, ASAM, EURETILE, PEPPHER)**	
14:45	0:25	**Coffee break**	Business Lounge	**Break + Demo**	
15:10	1:20		Auditorium	**Cluster 1 Session: Brainstorming (Smecy, iFEST, 2Parma, ALMA, Faster, Reflect, Madness)**	
			Business Lounge	**Cluster 2 Session: Brainstorming (ERA, DeSyRe, EPICS, ASAM, EURETILE, PEPPHER)**	
16:30	1:00	**Plenary session**	Business Lounge	**Drinks + informal discussion outcome of brainstorm**	Final comments by: G. Kuzmanov
17:30	1:00	**Reception**	Business Lounge		
18:30		**End of day**			

Tuesday

Time	Duration	Section	Room	Title	Authors
8:00	1:00	**Registration**	Hallway		
9:00	0:45	**Keynote 2**	Auditorium	**Application-driven FPGA-based Supercomputing: Janus and Janus2**	Lele Tripiccione
9:45	2:30	**Advances in Arithmetic**			
9:45	0:25		Auditorium	**(M,p,k)-friendly points: a table-based method for trigonometric function evaluation**	Nicolas Brisebarre, Milos Ercegovac and Jean-Michel Muller
10:10	0:25		Auditorium	**On-line decimal adder with RBCD representation**	Carlos Garcia Vega, Sonia Gonzalez Navarro, Julio Villalba Moreno and Emilio Lopez
10:35	0:50	**Coffee break**	Business Lounge	**Break + Poster Session II**	
11:25	0:25		Auditorium	**Virtual Floating-point Units for Low-power Embedded Processors**	Syed Gilani, Nam Kim and Michael Schulte
11:50	0:25		Auditorium	**Simultaneous floating-point sine and cosine for VLIW integer processors**	Claude-Pierre Jeannerod and Jingyan Jourdan-Lu
12:15	1:05	**Lunch**	Business Lounge		
		Digital Signal Processing Applications			
13:20	0:25		Auditorium	**A High-Rate, Low-Power, ASIC Speech Decoder Using Finite State Transducers**	Jeff Johnston and Rob Rutenbar
13:45	0:25		Auditorium	**Partial Expansion Graphs: Exposing Parallelism and Dynamic Scheduling Opportunities for DSP Applications**	George Zaki, William Plishker, Shuvra Bhattacharyya and Frank Fruth
14:10	0:25		Auditorium	**SIMD/MIMD dynamically-reconfigurable architecture for high-performance embedded vision systems**	A. Nieto, D.L. Vilariño, and V.M. Brea
14:35	0:50	**Coffee break**	Business Lounge	**Break + Poster Session III**	
15:25	2:35	**Free time**			
18:00	1:30	**Tour of Delft**	Market		
19:30	2:30	**Conference Dinner**	van der Dussen		
22:00		**End of day**			

Wednesday					
Time	**Duration**	**Section**	**Room**	**Title**	**Authors**
9:00	0:45	**Keynote 3**	Auditorium	**Designing Ultra Low Power SIMD Processors**	Henk Corporaal
		Cryptology and Security			
9:45	0:25		Auditorium	**A Speed Area Optimized Embedded Co-processor for McEliece Cryptosystem**	Santosh Ghosh, Jeroen Delvaux, Leif Uhsadel, and Ingrid Verbauwhede
10:10	0:25		Auditorium	**Interface design for mapping a variety of RSA exponentiation algorithms on a HW/SW co-design platform**	Leif Uhsadel, Markus Ullrich, Ingrid Verbauwhede and Bart Preneel
10:35	0:25		Auditorium	**Instruction Set Extensions for Cryptographic Hash Functions on a Microcontroller Architecture**	Jeremy Constantin, Andreas Burg and Frank K. Gürkaynak
11:00	0:50	**Coffee break**	Business Lounge	**Break + Poster Session IV**	
		Application-specific Acceleration			
11:50	0:25		Auditorium	**Design Automation Framework for Application-Specific Logic-in-Memory Blocks**	Qiuling Zhu, Kaushik Vaidyanathan, Ofer Shacham, Mark Horowitz, Larry Pileggi and Franz Franchetti
12:15	0:25		Auditorium	**Viterbi Accelerator for Embedded Processor Datapath**	Muhammad Waqar Azhar, Magnus Själander, Hasan Ali, Akshay Vijayashekar, Tung Thanh Hoang, Kashan Khurshid Ansari and Per Larsson-Edefors
12:40	0:25		Auditorium	**Accelerating NoC-based MPI Primitives via Communication Architecture Customization**	Libo Huang, Zhiying Wang and Nong Xiao
13:05		**End of Conference**			
		Posters	**Session**	**Title**	**Authors**
			I	**A Linear Algebra Core Design For Efficient Level-3 BLAS**	Ardavan Pedram, Syed Gilani, Nam Sung Kim, Robert Van De Geijn, Michael Schulte and
			I	**Reconfigurable Cluster-based Networks-on-Chip for Application-specific MPSoCs**	Mehdi Modarressi and Hamid Sarbazi-Azad
			I	**Automated synthesis of FSMD-based accelerators for hardware compilation**	Nikolaos Kavvadias and Kostas Masselos
			I	**Design Space Exploration for the Implementation of a Predictive Current Controller based on FPGA**	Pedro Martín, Osmell Machado, Francisco J. Rodríguez and Emilio J. Bueno
			II	**Design of Low Power On-Chip Processor Arrays**	Vahid Lari, Shravan Muddasani, Srinivas Boppu, Frank Hannig and Jürgen Teich
			II	**Novel Application of Genetic Sequencing Algorithms to Optimization of Hardware Resource Sharing for DSP**	Stephen McKeown and Roger Woods
			II	**Enabling Automatic Pipeline Utilization Improvement in Polyhedral Process Network Implementations**	Sven van Haastregt and Bart Kienhuis
			III	**Long Residue Checking for Adders**	Michael Sullivan and Earl Swartzlander
			III	**FPGA based Particle Identification in High Energy Physics Experiments**	Fatih Ugurdag, Ali Basaran, Taylan Akdogan, Ugur Guney and Sezer Gören
			III	**Real-Time Iris Segmentation on FPGA**	Hau Ngo, Jennifer Shafer, Robert Ives, Ryan Rakvic and Randy Broussard
			IV	**Reconfigurable design automation by high-level exploration**	Tim Todman and Wayne Luk
			IV	**MARTHA: A Multicore Architecture for Control and Emulation of Powe**	Michel Kinsy
			IV	**Exploiting FPGA-Aware Merging of Custom Instructions for Runtime R**	Siew Kei Lam, Thambipillai Srikanthan and Christopher T. Clarke